Remarks/Arguments

Claims 1-7 and 9-26 remain in this application. Claims 33-37 have been added.

Rejections Under 35 U.S.C. 102(b)

The Examiner has rejected claims 1, 2, 5, 6, 7, 9-12, 15-19, 22-24, and 26 under 35 U.S.C. 102(b) for alleged anticipation by Kitsukawa *et al.* (U.S. Patent No. 5,844,853).

Analysis

For anticipation to be found under 35 U.S.C. 102(b), every element of the claimed invention must be disclosed in the prior art document explicitly or inherently. The disclosure must show the identical invention in as complete detail as is contained in the claim, and the elements must be arranged as required by the claim. Applicant submits that this requires that the disclosure not be one which merely mentions piecewise and scattered throughout the document each major constituent element of the claim, i.e. each apparatus component and/or method step, in an unrelated manner. Applicant submits that anticipation requires that the prior art document disclose the claimed invention in its entirety, and hence must disclose, explicitly or inherently, all of the constituent elements, along with their particular arrangement, combination, functionality and interrelationships.

Claims 1, 2, 5, 6, 7, 9-12, 15-16

With respect to claim 1, the Examiner has alleged that Kitsukawa *et al.* discloses "a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second signal conditioning circuit for other than for performing the second signal conditioning function and for use by the second signal conditioning circuit during operation thereof" and relies on Figures 3a and 3b and the passage found at column 3, line 55 to column 4, line 8 of Kitsukawa *et al.* for that assertion.

In paragraph 3 of the Office Action, the Examiner has equated the first integrated semiconductor die of claim 1 with element **8a**, the 3.3V version of the DRAM of Kitsukawa *et al.*, has equated the second integrated semiconductor die of claim 1 with the element **8b**, the 2.5V version of the DRAM of Kitsukawa *et al.*, has equated the first ancillary circuit of claim 1 with the element **22**, the first voltage regulator of the 3.3V version of the DRAM of Kitsukawa *et al.*, and has equated the second ancillary circuit of claim 1 with the element **24**, the second voltage regulator of the 3.3V version of the DRAM of Kitsukawa *et al.*

The Examiner has stated in response to Applicant's arguments filed 1/29/09 that the Examiner "sees no distinction between having two separate chips that are later formed to be on the *same* supporting substrate where they are electrically connected, as Applicant claims, versus a device that is made to performed[sic] separate devices that are electrically connected to the same supporting substrate."

Applicant makes no statement as to whether or not there is any distinction, in the words of the Examiner, "between having two separate chips that are later formed to be on the *same* supporting substrate where they are electrically connected" versus "a device that is made to performed[sic] separate devices that are electrically connected to the same supporting substrate".

Furthermore, Applicant makes no statement as to whether or not a hypothetical claim attempting to claim broadly the subject matter of the general limitation the Examiner has alleged Applicant has claimed, namely, "two separate chips that are later formed to be on the *same* supporting substrate where they are electrically connected", would be anticipated or patentable over Kitsukawa *et al.* or otherwise. Applicant should like to strongly point out, however, that the specific claims at issue are not attempting to claim broadly the subject matter of the general limitation of said hypothetical claim as alleged by the Examiner.

Applicant respectfully submits that Kitsukawa *et al.* does not disclose, teach, or suggest "a *second ancillary circuit* integrated within the *first integrated circuit* semiconductor die and electrically coupled to the second signal conditioning circuit *for other than for performing the second signal conditioning* function and *for use by the second signal conditioning circuit during operation thereof.*"

The passages and figures of Kitsukawa *et al.* relied upon by the Examiner clearly show that the voltage regulator **24** of the 3.3V device **8a** is used to supply peripheral voltage (V_{PERI}) for the peripheral circuits **10** of the 3.3V device **8a**. As such, voltage regulator **24** of the 3.3V version of the device **8a** *does not perform any function for use by any circuit* of the 2.5V device **8b**. Moreover, the passage found at column 4, lines 26-38 of Kitsukawa *et al.* describes how the voltage regulator **24** in the 2.5V version of the device **8b** is completely bypassed and unused since the voltage of V_{PERI} in the 2.5V version of the device is the same as V_{DD} (2.5V) and hence can be supplied by V_{DD} directly.

It is clear from the aforementioned passages of Kitsukawa *et al.*, that the circuit of Kitsukawa *et al.* which the Examiner has asserted as being equivalent to the second ancillary circuit of claim 1, namely, voltage regulator **24**, is used in the 3.3V device **8a** only to supply voltage to circuits located on *the same device which the examiner has equated with an IC die*, and is simply not used at all in the 2.5V device **8b**.

Kitsukawa *et al.* simply does not disclose, teach, or suggest *any* circuit element of the 3.3V device **8a** (let alone the voltage regulator **24**) being for use by *any* circuit element of the 2.5V device **8b** nor does it disclose, teach, or suggest *any* circuit element of the 2.5V device **8b** (let alone the bypassed and unused voltage regulator **24**) being for use by *any* circuit element of the 3.3V device **8a**.

For at least the foregoing reasons, Applicant submits that the Examiner has not shown that Kitsukawa *et al.* discloses, teaches, or suggests "a *second ancillary circuit* integrated within the *first integrated circuit* semiconductor die and electrically coupled to the second

signal conditioning circuit *for other than for performing the second signal conditioning* function and *for use by the second signal conditioning circuit during operation thereof.*" Moreover, claim 1 has been amended to recite that the electronic apparatus comprises a first integrated circuit semiconductor die "of a *first semiconductor technology*" and a second integrated circuit semiconductor die "of a *second semiconductor technology physically different from the first semiconductor technology*". Applicant submits that the amendments to claim 1 do not constitute the addition of any new subject matter, and are fully supported throughout the specification as originally filed.

Applicant respectfully submits that Kitsukawa *et al.* does not disclose, teach, or suggest in combination with the limitations discussed hereinabove, the limitations that the first integrated circuit semiconductor die is "of a *first semiconductor technology*" and the second integrated circuit semiconductor die is "of a *second semiconductor technology physically different from the first semiconductor technology*".

With these amendments, claim 1 specifically recites, amongst other elements, two circuits, one circuit (second ancillary circuit) for use by another circuit (second signal conditioning circuit), and moreover, that the one circuit and the another circuit are integrated in separate integrated circuit semiconductor dies which are *of physically different semiconductor technologies.*

Kitsukawa *et al.* simply does it disclose, teach, or suggest that any circuit of the 3.3V device **8a** or the 2.5V device **8b** is for use by a circuit of the other device and that these two devices are of *physically different semiconductor technologies.*

For at least all of the foregoing reasons Applicant submits that Kitsukawa *et al.* does not disclose, teach, or suggest "a *second ancillary circuit* integrated within the *first integrated circuit* semiconductor die and electrically coupled to the second signal conditioning circuit *for other than for performing the second signal conditioning* function and *for use by the second signal conditioning circuit during operation thereof*" nor that in addition thereto

that the integrated circuit semiconductor die is "of a *first semiconductor technology*" and that the second integrated circuit semiconductor die is "of a *second semiconductor technology physically different from the first semiconductor technology*".

Applicant submits, therefore, that claim 1 is not anticipated by Kitsukawa *et al.* and respectfully requests that the Examiner withdraw the 35 U.S.C. 102(b) rejection thereof.

For at least the reason that claim 1 is not anticipated by Kitsukawa *et al.*, Applicant submits that claims 2, 5, 6, 7, 9-12, and 15-16 which depend from claim 1 are also not anticipated by Kitsukawa *et al.* and respectfully requests that the Examiner withdraw the 35 U.S.C. 102(b) rejections thereof.

Claims 17-19, 22-24 and 26

With respect to claim 17, the Examiner in paragraph 3 of the Office Action alleged that Kitsukawa *et al.* discloses the semiconductor apparatus as claimed in claim 17, using the same reasoning the Examiner applied to claim 1, discussed hereinabove in respect thereto.

Claim 17 has been amended in a similar manner as claim 1 has been amended, namely, to specifically recite that the electronic apparatus comprises a first integrated circuit die "of a *first semiconductor technology*" and a second integrated circuit die "of a *second semiconductor technology physically different from the first semiconductor technology*". Applicant submits that the amendments to claim 17 do not constitute the addition of any new subject matter, and are fully supported throughout the specification as originally filed.

Insofar as the reasoning applied by the Examiner equally applies to both claims 1 and 17, so also do Applicant's submissions hereinabove apply equally to claims 1 and 17. Applicant submits therefore, that for at least all of the reasons given hereinabove that Kitsukawa *et al.* does not disclose, teach or suggest all of the features of claim 1, that Kitsukawa *et al.* does not disclose, teach or suggest all of the features of claim 17.

Applicant submits, therefore, that claim 17 is not anticipated by Kitsukawa *et al.* and respectfully requests that the Examiner withdraw the 35 U.S.C. 102(b) rejection thereof.

For at least the reason that claim 17 is not anticipated by Kitsukawa *et al.*, Applicant submits that claims 18-19, 22-24, and 26 which depend from claim 17 are also not anticipated by Kistukawa *et al.* and respectfully requests that the Examiner withdraw the 35 U.S.C. 102(b) rejections thereof.

Rejections Under 35 U.S.C.102(b)/35 U.S.C. 103(a)

The Examiner has rejected claims 3, 4, 8, 13, 14, 20, 21, and 25 under section 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) for allegedly being obvious over Kitsukawa *et al.* (U.S. Patent No. 5,844,853).

Analysis

The Examiner has relied upon the reasons given in respect of claims 1 and 17, stating in paragraph 21 of the Office Action, "Kitsukawa discloses the semiconductor device substantially as claimed. Please see above rejection."

Insofar as the reasoning applied by the Examiner in the "above rejection" to show "Kitsukawa discloses the semiconductor device substantially as claimed" equally applies to the anticipation rejections as it does to the rejection on the basis of anticipation by or, in the alternative on the basis of obviousness of claims 3, 4, 8, 13, 14, 20, 21, and 25, so also do Applicant's submissions hereinabove, which show that Kitsukawa in fact does not disclose the semiconductor device substantially as claimed, equally apply to the anticipation rejections as they do to the rejection on the basis of anticipation by or, in the alternative on the basis of obviousness of claims 3, 4, 8, 13, 14, 20, 21, and 25.

As submitted in great detail hereinabove, Kitsukawa *et al.* simply does not disclose, teach, or suggest all of the features of each of independent claims 1 and 17, and hence Applicant

respectfully submits that the Examiner has not shown a *prima facie* case of obviousness against either of amended claims 1 or 17, and respectfully requests that the Examiner withdraw the 35 U.S.C. 103(a) rejections of claim 1 and 17.

Moreover, Applicant submits that the common general knowledge of a person skilled in the art combined with the teachings of Kitsukawa *et al.* which are examples thereof, in the absence of hindsight and the knowledge presented in the description of the present application, teach away or at the least "suggest away" from the subject matter of claims 1 and 17.

The advantages of integrating ancillary circuits on the *same die* as the circuits they support are widely and well known to persons skilled in the art, and as such all first attempts to integrate an ancillary circuit into a design would be to integrate it on the same die as the circuit it supports. Barring that choice, the necessary drawbacks involved with having to put ancillary circuits onto a separate module, when the die in which the circuit it supports is unsuitable for integration of the ancillary circuit are accepted and known drawbacks which accompany the common practice, Applicant submits, of accommodating the ancillary circuit on *additional and specialized dies to house the supporting circuitry.* Applicant submits that in light of the description of Kitsukawa *et al.* and common general knowledge in the art, a person of ordinary skill in the art would *not* have incorporated into an electronic apparatus *integration of an ancillary circuit on a die different from the one which houses a circuit it supports* and which already has signal conditioning circuitry *which the ancillary circuit does not support.*

For at least the reason that claims 1 and 17 are not unpatentable over Kitsukawa *et al.*, Applicant submits that claims 3, 4, 8, 13, 14, 20, 21, and 25 which depend from one of claims 1 and 17 are also not unpatentable over Kistukawa *et al.* and respectfully requests that the Examiner withdraw the 35 U.S.C. 103(a) rejections thereof.

Further amendments to the claims

In addition to the claim amendments that have been described above, claim 1 has been amended to correct typographical errors, claims 3, 4, 7, and 11-14 have been amended for consistency with the amendments made to claim 1, claim 15 has been amended to correct typographical errors, claims 20, 21, 24, and 25 have been amended for consistency with the amendments made to claim 17, and claim 26 has been amended to correct typographical errors.

Claim 8 has been cancelled.

Claims 33- 37 have been added to claim subject matter directed to why the second ancillary circuit is integrated in the first integrated circuit die. Applicant submits that the addition of these new claims does not constitute the addition of any new subject matter, and that the subject matter thereof is fully supported throughout the specification as originally filed, and more particularly by paragraphs [006] and [0033] of the specification as originally filed.

Amendments to the Specification

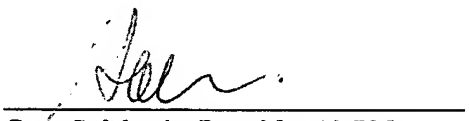
Amendments to paragraphs [004], [006], [025], and [033] have been made to correct typographical errors.

Applicant submits that for at least all of the foregoing reasons that the amended claims are in allowable form, that the application is in condition for allowance.

Applicant respectfully requests favorable consideration.

Please charge any additional fees required or credit any overpayment to Deposit Account No. 20-1430.

Respectfully submitted,



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